at least one of the selecting switch sections comprise:

a buffer section for receiving delayed input signal from one of the delay stages;

a selecting section directly connected to the buffer section for activating the buffer section to establish the delay path; and

selecting means for establishing a delay path for the input signal by selecting one of the selecting switch sections, wherein

an output signal from the delay path has a desired delay time.

26. (Amended) A semiconductor integrated circuit device comprising:

a delay section having two or more predetermined delay stages, each predetermined delay stage adds a predetermined delay time to an input signal;

selecting switch sections, wherein at least one of the selecting switch sections comprise:

a buffer section for receiving delayed input signal from one of the delay stages; and

a selecting section directly connected to the buffer section for activating the buffer section to establish the delay path; and

selecting means for establishing a delay path for the input signal by selecting one of the selecting switch sections, and wherein an output signal from the delay path has a desired delay time.

29. (Twice Amended) A delay method comprising:

a delay step in which predetermined delay times are sequentially added onto an input signal to obtain delay signals;

a selecting step which is activated to obtain one of the delay signals in the delay step which has a desired delay time; and

an output step in which one of the delay signals in the delay step is output by activating the selecting step.

A marked-up copy of the amended claims is attached as required under 37 CFR §1.121.

Please add claim 32 as follows:

32. (New) A delay circuit comprising:

a delay section having two or more predetermined delay stages each of which is provided with an individual delay input terminal for inputting a signal to which predetermined delay time is added, the signal inputted to each predetermined delay stage having substantially uniform rise delay time and all delay time, and

selecting switch sections, each of the selecting switch sections comprising:

a buffer section provided for each individual delay input terminal with an output terminal of the buffer section being connected to the individual delay input terminal and input terminals of entirely of buffer sections being mutually joined:

a selecting section directly connected to the buffer section for activating the buffer section to establish a delay path; and